AF/Blum

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

AMITABH JAIN ET AL.

Serial No. 10/816,776 (TI-34913AA)

Filed April 2, 2004

For: ULTRA SHALLOW JUNCTION FORMATION

Art Unit 2813

Examiner David S. Blum

Customer No. 23494

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Jay M. Cantor, Reg. No. 19,906

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P. O. Box 1450
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Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 18, all of the rejected claims. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

A non-amending response was filed after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a method for forming ultra shallow junctions in a semiconductor substrate. In accordance with the method, a dopant species is implanted into the semiconductor substrate with the implanted region being made amorphous either prior to or subsequent to the implant. An low temperature anneal takes place to crystallize the amorphous region and than a second annealing of the implanted semiconductor substrate takes place with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C for a period of from 0.5 to 3 milliseconds.

GROUNDS OF REJECTION

Claims 1 to 18 were rejected under 35 U.S.C. 102(e) as being anticipated by Mayur (U.S. 2003/0040130A1).

ARGUMENT

Claims 1 to 18 were rejected under 35 U.S.C. 102(e) as being anticipated by Mayur (U.S. 2003/0040130A1). The rejection is without merit.

It is basic that for a claim to be anticipated under 35 U.S.C. 102, a single reference must contain each and every feature claimed as well as the function claimed of each feature. This is clearly not the case herein.

Claim 1 requires, among other features, the step of annealing the implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C. Mayur teaches an implant anneal at a temperature of greater than 1300K which as about 1026C. In the Office action dated 3/29/2005, the examiner states, "the examiner finds that a teaching of a temperature above 1026 C., suggests a temperature of at least 1050 C., thus teaching at least one temperature within the range." There is no basis for the examiner to arrive at this conclusion. There is nothing in the cited reference that would lead the examiner to interpret, "a temperature above 1026 C" as suggesting a temperature of at least 1050 C. The above statement means exactly what it describes. It clearly means temperatures above 1026 C which includes 1027 C, 1028 C etc. Clearly a temperature of a million degrees C or ten thousand degrees C could not be an operating temperature for semiconductor fabrication. It follows that the open-ended temperature in Mayur is not unlimited and therefore cannot be equated to the range claimed in claim 1 but for a first reading of the subject disclosure. It follows that the examiner's conclusion that the above statement means a temperature of at least 1050 C is clearly erroneous and improper. The claimed temperature range of 1050 – 1350 degrees C is not disclosed or even suggested in the cited reference. It follows that the rejection under section 102 is not supported.

The above argument applies to all of the rejected claims, each of which contains the above-discussed limitation.

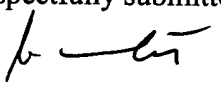
Claims 4, 6 10 and 14 further limits the claims from which they depend by requiring that the anneal take place for a period of from 0.5 to 3 seconds. No such range is found in Mayur. A time period of "less than 50 mS" in paragraph [00007] does not teach the claimed range. Clearly, less than 50 could include zero which is clearly not contemplated by Mayur. It follows that there must be some unspecified lower limit and there is no reason to extend this lower limit to that claimed herein except by prior reference to the subject disclosure as a teaching. Clearly the time provide in paragraph [00009] of is not only out of the claimed range, but it refers to the recrystallization step and not to the high temperature anneal.

The cited reference in paragraphs 0077 and 0083 describe the need to use the thermal properties of amorphous silicon in numerical modeling. Representative values of these thermal properties are given in Table II. The heading for table II of, "[T]hermal parameters for amorphous silicon used..." further supports this conclusion. The melting temperature of 1423 K given in Table II is therefore a property of the amorphous silicon used rather than an annealing. The examiner's interpretation of the 1423 K temperature given in Table II is erroneous and improper.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



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CLAIMS APPENDIX

The claims on appeal read as follows:

1. A method for forming ultra shallow junctions, comprising:

providing a semiconductor;

implanting a dopant species into said semiconductor; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C.

2. The method of claim 1 further comprising an amorphizing implant.

3. The method of claim 2 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

4. The method of claim 1 wherein said ultra high temperature anneal comprises times from 0.5 milliseconds to 3 milliseconds.

5. A method for forming junction in integrated circuits, comprising:

providing a semiconductor;

forming a patterned photoresist layer on said semiconductor;

implanting dopant species into said semiconductor;

removing said patterned photoresist layer;

annealing said implanted semiconductor with a solid phase epitaxy anneal; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C.

6. The method of claim 5 wherein said ultra high temperature anneal comprises times from 0.5 milliseconds to 3 milliseconds.

7. The method of claim 6 further comprising an amorphizing implant.

8. The method of claim 7 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

9. A method of forming a MOS transistor, comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

implanting dopant species into said semiconductor adjacent to said gate electrode;

annealing said implanted semiconductor with a solid phase epitaxy anneal at a temperature between 550°C and 950°C; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C.

10. The method of claim 9 wherein said ultra high temperature anneal comprises times from 0.5 milliseconds to 3 milliseconds.

11. The method of claim 10 further comprising an amorphizing implant performed prior to said implanting of said dopant species.

12. The method of claim 11 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

13. A method of forming an integrated circuit MOS transistor, comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

implanting first dopant species into said semiconductor adjacent to said gate electrode;

forming sidewall structures adjacent to said gate electrode;

implanting second dopant species into said semiconductor adjacent to said sidewall structures; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C.

14. The method of claim 13 wherein said ultra high temperature anneal comprises times from 0.5 milliseconds to 3 milliseconds.

15. The method of claim 14 further comprising an amorphizing implant performed prior to said implanting of said first dopant species.

16. The method of claim 15 further comprising an amorphizing implant performed prior to said implanting of said second dopant species.

17. The method of claim 13 further comprising an amorphous implant performed prior to said implanting of said second dopant species.

18. The method of claim 16 wherein said amorphizing implants comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None